Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-16. (canceled)

17. (currently amended): A method of manufacturing a non-volatile semiconductor memory device, comprising ~~the steps of~~:

forming, on a first region of a semiconductor substrate, a self-aligned double-layer gate structure which includes a gate insulating film, a first conductor serving as a floating gate layer, a second conductor serving as a control gate layer, and an insulating film electrically insulating the first and second conductors,

patterning the first conductor into a gate electrode of a transistor above a second region of the semiconductor substrate; and

providing a third conductor on the first conductor patterned in ~~the~~ a form of the gate electrode above the second region.

18. (currently amended): A method of manufacturing a non-volatile semiconductor memory device, comprising ~~the steps of~~:

sequentially forming, on a semiconductor substrate, a gate insulating film, a first conductor serving as a floating gate layer, an insulating film, and a second conductor serving as a control gate layer;

patterning the second conductor, the insulating film and the first conductor in a self-aligned manner in a first region of the semiconductor substrate, using a single mask, thereby forming a double-layer gate structure, and removing that portion of the second conductor which is provided on a second region of the semiconductor substrate during the patterning of the second conductor in the first region;

forming a third conductor on the first conductor in the second region after the patterning of the first conductor in the first region, such that the first and third conductors are electrically connected to each other; and

patterning the third and first conductors into a gate electrode of a transistor in the second region.

19. (currently amended): A method of manufacturing a non-volatile semiconductor memory device, according to claim 17, further comprising ~~the steps of~~ forming an element isolating region adjacent to the transistor, and forming the double-layer gate structure on the element isolating region.

20. (currently amended): A method of manufacturing a non-volatile semiconductor memory device, according to claim 18, further comprising ~~the steps of~~ forming an element isolating region adjacent to the transistor, and forming the double-layer gate structure on the element isolating region.